LESSON PLAN

Subject Code & Name: 13EC3021 & VLSI DESIGN

Branch: E.C.E-A

Class / Semester: III/II Academic Year:2016-17

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| Period | date | Topic | Unit No. | Teaching Methodology | Remarks | Corrective action upon review |
|  |  | Introduction: | I |  |  |  |
| 1 | 5/12/16 | Introduction to IC technology |  | PPT |  |  |
| 2 | 7/12/16 | The IC era, MOS and related VLSI technology and basic MOS transistors |  | PPT |  |  |
| 3-9 | 7,8,12,14,14,15,19/12/16 | IC production process, |  | PPT |  |  |
| 10-12 | 21/12/16 | MOS and CMOS fabrication process |  | PPT |  |  |
| 13 | 22/12/16 | Bi-CMOS technology |  | PPT |  |  |
| 14 | 26/12/16 | Comparison between CMOS and bipolar technologies. |  | PPT |  |  |
|  |  | Basic electrical properties of MOS and Bi-CMOS circuits : | II |  |  |  |
| 15 | 28/12/16 | Ids – Vds relationship |  | CR |  |  |
| 16 | 28/12/16 | Aspects of MOS transistor: threshold voltage, trans-conductance, output conductance and figure of merit |  | CR |  |  |
| 17 | 29/12/16 | Pass transistor, MOS inverter, |  | CR |  |  |
| 18 | 2/1/17 | Determination of pull-up to pull-down ratio of NMOS. |  | CR |  |  |
| 19 | 4/1/17 | NMOS inverter driven by another NMOS inverter and driven through one or more pass transistors |  | CR |  |  |
| 20 | 4/1/17 | Alternative forms of pull-up, |  | CR |  |  |
| 21 | 5/1/17 | CMOS inverter |  | CR |  |  |
| 22  23 | 9/1/17  11/1/17 | MOS transistor circuit model, Bi-CMOS inverter and latch-up in CMOS circuits. |  | CR |  |  |
|  |  | VLSI Circuit design process | III |  |  |  |
| 24 | 23/1/17 | VLSI design flow |  | PPT |  |  |
| 25-26 | 25/1/17 | Layers of abstraction and stick diagrams Design rules for wires, contacts |  | PPT |  |  |
| 27-30 | 30/1/17  1,2/2/17 | Transistor layout diagrams for NMOS and CMOS inverters and gates |  | PPT |  |  |
|  |  | Scaling of MOS circuits: |  |  |  |  |
| 31 | 6/2/17 | Scaling models |  | PPT |  |  |
| 32-34 | 8,9/2/17 | Scaling factors for device parameters and limitations of scaling. |  | CR |  |  |
|  |  | Gate level design: | IV |  |  |  |
| 35 | 9/2/17 | Logic gates and other complex gates |  | CR |  |  |
| 36 | 13/2/17 | Switch logic |  | CR |  |  |
| 37-38 | 15/2/17 | Alternate gate circuits. |  | CR |  |  |
|  |  | Basic circuit concepts: |  |  |  |  |
| 39 | 16/2/17 | Sheet resistance (Rs) and its concept to MOS |  | CR |  |  |
| 40-41 | 20,22/2/17 | Area capacitance calculations, |  | CR |  |  |
| 42 | 27/2/17 | Delays, |  | CR |  |  |
| 43 | 6/3/17 | Driving large capacitive load, wiring capacitances |  | CR |  |  |
| 44 | 8/3/17 | Fan-in and fan-outs and choice of layers |  | CR |  |  |
|  |  | Subsystem design: |  |  |  |  |
| 45 | 8/3/17 | Shifters |  | PPT |  |  |
| 46 | 15/3/17 | Adders |  |  |  |  |
| 47 | 15/3/17 | ALUs |  | PPT |  |  |
| 48 | 16/3/17 | Multipliers |  | PPT |  |  |
| 49 | 20/3/17 | Parity generators. |  | PPT |  |  |
|  |  | Design methods: | V |  |  |  |
| 50-51 | 22,23/3/17 | Design-capture tools |  | CR |  |  |
| 52 | 27/3/17 | Design- verification tools |  | CR |  |  |
|  |  | Cmos testing: |  |  |  |  |
| 53 | 29/3/17 | Need for CMOS testing |  | CR |  |  |
| 54 | 30/3/17 | Manufacturing test principles |  | CR |  |  |
| 55 | 3/4/17 | Design strategies for test |  | CR |  |  |
| 56 | 6/4/17 | Chip level test techniques |  | CR |  |  |
| 57 | 10/4/17 | System level test techniques. |  | CR |  |  |